S/N Unknown **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Kie Y. Ahn et al.	Examiner: Unknown
Serial No.:	Unknown	Group Art Unit: Unknown
Filed:	Herewith	Docket: 303.678US3
Title:	STRUCTURE AND METHOD FOR DUAL GATE OXIDE THICKNESSES	

PRELIMINARY AMENDMENT

BOX PATENT APPLICATION
Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to taking up the above-identified patent application for examination, please amend the application as follows:

IN THE SPECIFICATION

On page 1, line 3, before the heading, "Field of the Invention", insert the following paragraph:

Cross Reference to Related Application(s)

This application is a division of U.S. Patent Application No. 09/514,629, filed on February 28, 2000, the specification of which is incorporated herein by reference.

IN THE CLAIMS

Please cancel claims 1 - 32 and 41 - 54, without prejudice or disclaimer, after adding the following new claims.

55. (New) A logic device and a memory device structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a top layer which exhibits a high resistance to oxidation at high temperatures; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness.

56. (New) The structure of claim 55, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

57. (New) The structure of claim 55, wherein first dielectric layer of a first thickness includes silicon dioxide (SiO_2) and the top layer includes silicon nitride (Si_3N_4).

58. (New) The structure of claim 55, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

59. (New) The structure of claim 55, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

60. (New) The structure of claim 55, wherein the top layer includes a top layer of silicon nitride (Si_3N_4) which comprises approximately a third of the first thickness of the first dielectric layer.

61. (New) The structure of claim 55, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.

62. (New) A logic device and a memory device structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a top layer which exhibits a high resistance to boron penetration at high temperatures; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness.

63. (New) The structure of claim 62, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

64. (New) The structure of claim 62, wherein first dielectric layer of a first thickness includes silicon dioxide (SiO_2) and the top layer includes silicon nitride (Si_3N_4).

65. (New) The structure of claim 62, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

66. (New) The structure of claim 62, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

67. (New) A logic device and a memory device structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a silicon nitride (Si_3N_4) top layer which exhibits a high resistance to oxidation at high temperatures; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness.

68. (New) The structure of claim 67, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

69. (New) The structure of claim 67, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

70. (New) The structure of claim 67, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

71. (New) The structure of claim 67, wherein the silicon nitride (Si_3N_4) top layer includes a silicon nitride (Si_3N_4) top layer with a thickness of approximately a third of the first thickness of the first dielectric layer.

72. (New) The structure of claim 67, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.

73. (New) A logic device and a memory device structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a top layer of approximately a third of the first thickness, which exhibits a high resistance oxidation at high temperatures; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness.

74. (New) The structure of claim 73, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.

75. (New) The structure of claim 73, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

76. (New) The structure of claim 73, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

77. (New) The structure of claim 73, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

78. (New) A logic device and a memory device structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a top layer which exhibits a high resistance to oxidation at high temperatures; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness of less than 12 nanometers (nm).

79. (New) The structure of claim 78, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.

80. (New) The structure of claim 78, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

81. (New) The structure of claim 78, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

82. (New) A logic device and a memory device structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a silicon nitride (Si_3N_4) top layer of approximately a third of the first thickness, which exhibits a high resistance to oxidation at high temperatures; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness of less than 12 nanometers (nm).

83. (New) The structure of claim 82, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.

84. (New) The structure of claim 82, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

85. (New) The structure of claim 82, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

86. (New) A logic device and a memory device structure on a single substrate formed by the method comprising:

forming a pair of transistor channel regions on the single substrate;

forming a pair of gate oxides to a first thickness on the pair of channel regions;

wherein forming the pair of gate oxides to a first thickness includes forming the pair of gate oxides to a thickness of less than 5 nanometers (nm) by krypton plasma generated atomic oxygen at approximately 400 degrees Celsius;

forming a thin dielectric layer on one of the pair of gate oxides, wherein the thin dielectric layer exhibits resistance to oxidation at high temperatures; and

forming the other of the pair of gate oxides to a second thickness.

REMARKS

Claims 1 - 32 and 41 - 54 are canceled without prejudice or disclaimer and claims 55 - 86 were added. Claims 33 - 40 and 55 - 86 are now pending in this application.

The specification is amended to add a cross reference to the prior application. No new matter is added by way of these amendments.

The application filing fee as calculated on the application transmittal sheet reflects the amendments to the claims described above.

The Applicant respectfully requests that the preliminary amendment described herein be entered into the record prior to examination and consideration of the above-identified application.

Respectfully submitted,

KIE Y. AHN ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6944

Date 8/30/01 By _____
David C. Peterson
Reg. No. 47,857

"Express Mail" mailing label number: EL709306976US
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